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RF POWER PERFORMANCE OF AN LDMOSFET ON FM BROADCAST BAND II POWER AMPLIFIER APPLICATIONS

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ABSTRACT
The performance, analysis, design, and evaluation of medium-voltage laterally diffused metal oxide semiconductor (LDMOS) transistors for band II applications up to 108 MHz is presented. Using an optimized N-LDMOS transistor, the current state of laterally diffused metal-oxide-semiconductor (LDMOS) technology, which for over ten years has been the preferred tool for RF power applications. LDMOS satisfies the needs for numerous Class AB applications. The performance per unit gate width has been found to decline with increasing width, even when RF transmitter power amplifiers employ larger transistors to deliver higher power. A field solver and circuit simulator are used in this work to identify the mutual inductance in the system as a primary reason for the performance deterioration in RF LDMOSFET power amplifiers. For RF power applications, laterally diffused metal-oxide-semiconductor (LDMOS) technology has been the preferred device for more than ten years. LDMOS meets the specifications for a variety of Class AB and pulsed applications, including broadcast, microwave, and base station. We demonstrate the LDMOS transistor's cutting-edge RF performance using a load-pull test system, attaining class-AB drain efficiencies of 80% at FM broadcast band II , 88-108 MHz for both packaged and on-wafer devices. Additionally, the outcomes of a number of Class AB amplifier implementations built using this method are displayed.
***Index Terms*:** RF amplifiers, LDMOS Technology, microwave, semiconductor, Power Amplifier, Class AB Amplifier

I INTRODUCTION

This paper presents a laterally diffused metal-oxide-semiconductor (LDMOS) technology, which has been the device of choice for RF power applications for more than one decade. LDMOS fulfils the requirements for a wide range of Class AB applications, which lead to high-power amplifiers with increased bandwidth, efficiency, and gain (Seo and Zhang, 2019). The primary function of the power amplifier (PA), a crucial component of transmitter systems, is to raise the input signals' power level to a predetermined level. The criteria of PAs are mostly connected to the maximum efficiency and linearity performances, as well as the absolute attainable output power levels. Figure 1 depicts the physical structure of an LDMOS transistor. The LDMOS channel is predominately defined by the physical size of the gate structure. Laterally diffused metal-oxide-semiconductor (LDMOS) transistors were first introduced into the RF power market about 30 years ago as a replacement for bipolar transistors for RF power applications.

Figure 1. Selection of an LDMOS device

Over the past few decades, LDMOS has seen a dramatic improvement in RF performance and is currently the leading technology for a wide range of RF power applications in FM broadcastNumerous new opportunities are being explored, such as RF lighting and microwave cooking. The LDMOS frequency range of operation has expanded over the past few decades, currently covering a range from 1 MHz up to 4 GHz, including WiMAX and

band radar frequencies. LDMOS has a power range of over thirty years, with driver devices using a few watts and pulsed applications using several thousand watts.

Additionally, the integration of the RF power amplifier (PA) into a wireless system-on-a-chip, where all of the digital, analogue, and RF circuits of a wireless system are integrated onto a single die, may be possible with the use of an LDMOSFET in thin-film SOI. The development of a high-performance RF power device in thin-film SOI is acknowledged as being especially difficult, despite the fact that thin-film SOI is a promising technology platform for single-chip systems. A compound amplification using LDMOSFET on RF pallets board that performs well in comparison to bulk silicon LDMOSFETs is demonstrated in this research. This device fabricates the body contact underneath the source, which is essential to achieving a high breakdown voltage. This LDMOSFET's inherent performance is on par with or superior to that of any known RF power MOSFET. A promising technology platform for highly integrated, high-performance radio frequency circuits is THIN-FILM silicon-on-insulator (SOI). For these applications, it offers several benefits over bulk silicon, chief among them being the ability to employ a silicon substrate with a high resistivity. Both the active and passive components of an RF system benefit greatly from high resistivity cm silicon's reduction of substrate RF power loss. Although high resistivity bulk silicon is thought to provide reliability and yield issues, it provides the same RF performance benefits as high resistivity SOI. Digital logic and memory can be combined with high-performance radio frequency circuits on a single chip thanks to thin-film SOI made from a high-resistivity handle wafer and standard silicon.

The performance evolution is examined, together with the reliability and important improvement criteria. The performance of power LDMOS devices and a number of Doherty amplifiers over different frequency bands are summarized in this study. Among the examples are a 1500 W, 48 V LDMOS.

II. LDMOS DEVICE TECHNOLOGY

LDMOS (laterally diffused metal-oxide semiconductor) is a planar double-diffused MOSFET (metal–oxide–semiconductor field-effect transistor) used in amplifiers, including microwave power amplifiers, RF power amplifiers and audio power amplifiers (Najhart, 2016). Figure 2 displays an inner of RF LDMOSFET. P-type full-dose SIMOX wafers with an active silicon thickness of 200 nm, a buried oxide of 400 nm, and a resistivity of 10–20 cm were used to construct the partially depleted LDMOSFETs. Figure 3 shows the cross-section of an LDMOS module. The procedure was created to enable the integration of the SOI LDMOSFET into an SOI CMOS process. In mainstream SOI CMOS, the silicon thickness is equal to the film thickness. They employed LOCOS isolation". The slightly doped drain (LDD) region is 0.5 m, the gate oxide thickness is 30 nm, and the shortest n polysilicon gate is 0.7 m. To create the lateral body doping profile, the device's drain was covered, the source was implanted with boron of dose and energy 25 keV, and the wafers were annealed for 300 minutes at 1000°C. A phosphorus implant with an energy of 55 KeV and a dosage of cm produced the n LDD area. A masked implant with an energy of 25 keV and a dosage of cm created the source and drain zones. The length of the n region is defined by the n implant mask. Following processing, the n-junction depth beneath the source is 100 nm, while the silicon thickness beneath the gate is 180 nm.Figure 2 displays an inner of RF LDMOSFET. In mainstream CMOS, the silicon thickness is equal to the film thickness. The slightly doped drain (LDD) region is 0.5 m, the gate oxide thickness is 30 nm, and the shortest n polysilicon gate is 0.7 m. To create the lateral body doping profile, the device's drain was covered, the source was implanted with boron of dose and energy 25 keV, and the wafers were annealed for 300 minutes at 1000°C. A phosphorus implant with an energy of 55 KeV and a dosage of cm produced the n LDD area. A masked implant with an energy of 25 keV and a dosage of cm created the source and drain zones. The length of the n region is defined by the n implant mask. Following processing, the n-junction depth beneath the source is 100 nm, while the silicon thickness beneath the gate is 180 nm.

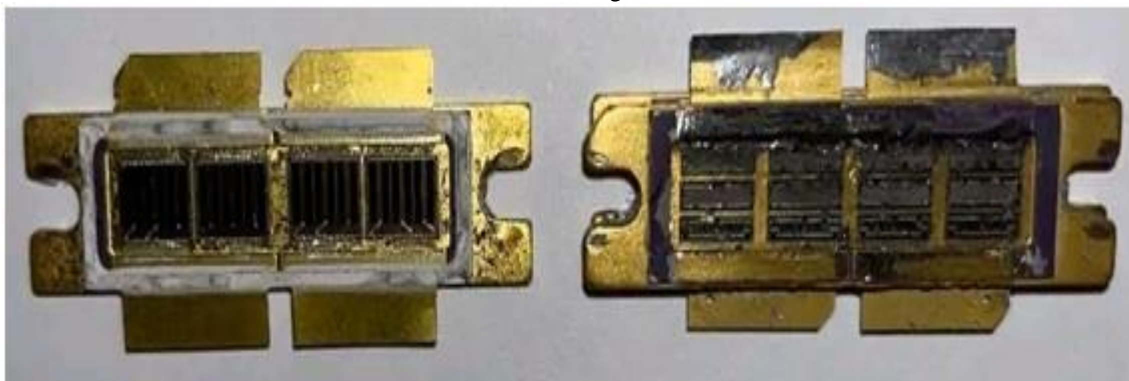

Figure 2. Photograph of an inner of RF LDMOSFET

The feasibility of applying the superjunction (SJ) concept to a thick-SOI LDMOS transistor for base station applications is studied in this paper. An extensive comparison with conventional RF LDMOS structures is performed in terms of breakdown voltage (VBR) versus drift resistance (Rdr) values (Cortes, 2006)

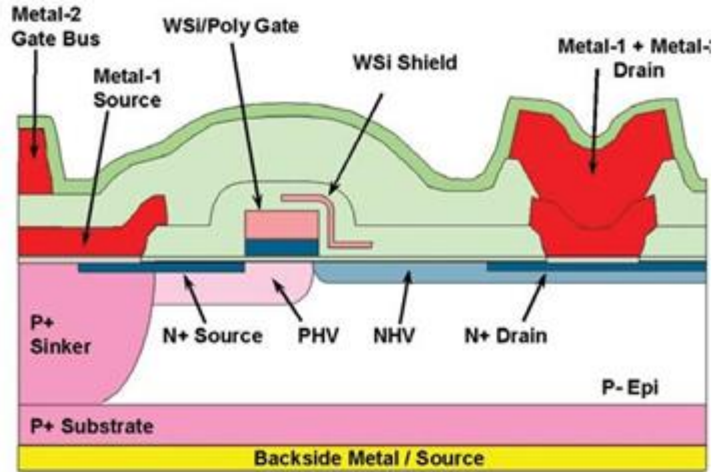

Figure 3. Cross Section of an LDMOS Module (Caverly,2015)

III Intrinsic LDMOS Performance

A. 28-V LDMOS RF Performance

A 28/32 V common-source, N-channel enhancement-mode, lateral field-effect, RF power transistor technology is used in the 28V BLF368 RF LDMOS module depicted in Figure 3. Our fabricated circuit at Peters A.O. Broadcasting Ado-Ekiti is specifically developed for broadband commercial, avionics, and industrial devices at frequencies up to 1.5 GHz for all common modulation formats, including Class A, AB, and C. Its output power ranges from 10 to 400 W.

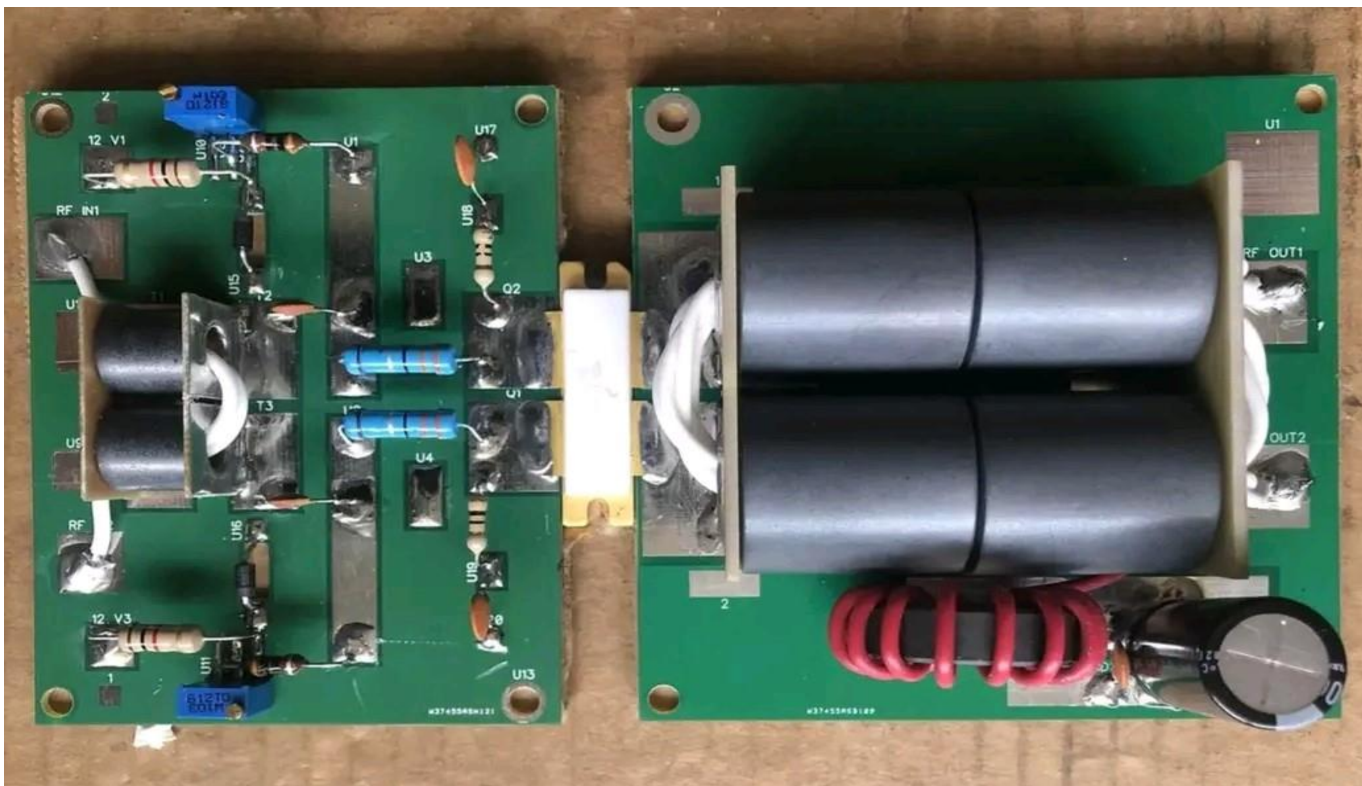

Figure 3. Photograph of 28V RF LDMOS Module

Figure 4 displays typical broadband performance in terms of power gain and efficiency versus output power at VDD=28 V. Typical broadband power amplifiers show good power gain and efficiency at VDD = 28V, particularly at higher output powers. While drain efficiency can range from 46% to 63%, power gain usually falls between 11.5 and 20 dB.

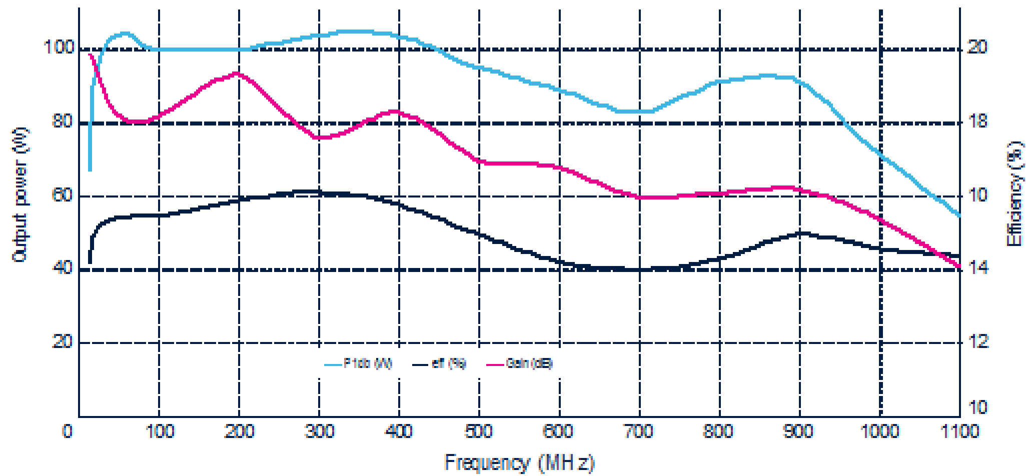

Figure 4. Power gain and efficiency versus output power at V_{DD}= 28 V

B. 48-V LDMOS RF Performance

A 48/50 V common-source, N-channel enhancement-mode, lateral field-effect, RF power transistor technology is used in the 48V BLF188XR RF LDMOS module depicted in Figure 5. Our fabricated circuit at Peters A.O. Broadcasting Ado-Ekiti is specifically developed for broadband commercial, avionics, and industrial devices at frequencies up to 1.5 GHz for all common modulation formats, including Class A, AB, and C. Its output power ranges from 10 to 1500 W.

Figure 5. Photograph of BLF188XR MOSFET

The Printed-Circuit Board (PCB) used has the specifications of RF 35; $\varepsilon_r = 3.5$; thickness = 0.765 mm; thickness copper plating = 35 µm, gold plated as layout shown in figure 6 "RF 35" is also intended for use in radio frequency applications. Its overall thickness is 0.765 mm, its dielectric constant (εr) is 3.5, and its copper plating layer is 35 microns thick with a gold plating finish. Applications needing longevity and high-frequency performance can use this board.

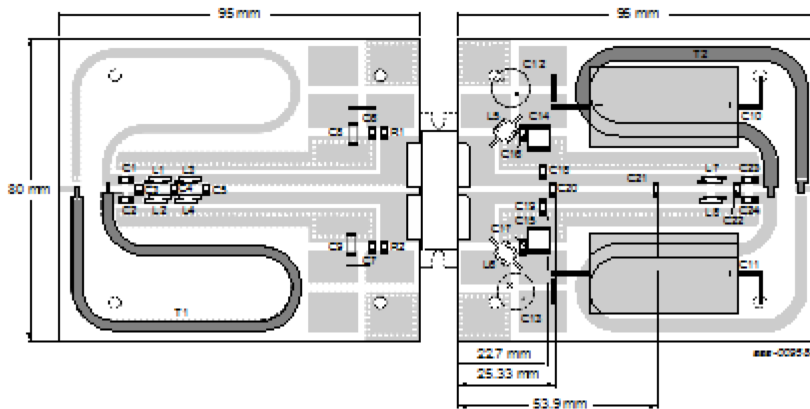

Figure 6. Printed-Circuit Board (PCB) used has the specifications of RF 35; $\varepsilon_r = 3.5$; thickness = 0.765 mm

Mechanical design and manufacturing had difficulties choosing materials, machining techniques, plating sequences, and constructing many crucial assemblies in order to match the new amplifier's RF design specifications. Figure 7 displayed the selection of materials was based on their mechanical and electrical qualities as well as their simplicity of production. When performing precision machining procedures, the designers had to use tubes, rods, or plates of varying diameters. With little deformation from clamping force, these formed raw materials are easily held in machines (lathe and mill) precisely. We employed the Metallurgy Characterisation Team of the Materials Science and Technology division's laboratories to assess the nickel and silver plating on a 6061 aluminium cylinder and plate test coupons in order to guarantee the plating quality from several sources.

The main points of interest were the electroless Ni's adherence to the base Al surface, the Ni and Ag plating's adhesion, and the thickness of the Ni and Ag plating. The FPA prototype team followed precise instructions based on calculations to complete the crucial assemblies of the G1 and G2 DC blocking capacitors and the filament bypass capacitor.

Figure 7. Mechanically design high power 48-V LDMOS

Special tools were employed, including as vacuum chambers to remove air from capacitor assemblies during potting/sealing operations, a kiln to heat parts, alignment fixtures for pressing and turntables to uniformly heat shrink dielectric sleeves. Device technology depends on RF power characteristics like bandwidth, efficiency, and power delivery. The RF power qualities offered by various device technologies differ, affecting things like signal quality and power usage. GaN-based devices provide greater efficiency at higher frequencies, although LDMOS devices are superior in power delivery as shown in the Table 1 below.

Table 1: Comparison of RF power attributes vs. device technology

Attribute	Si VMOS	28V RF-LDMOS	50V RF-LDMOS
CW eff. at P1dB	3	5	5
Power Gain	3	5	5
Thermal resistance	3	4	5
CW Packaged Power Density	3	3	4
High Intrinsic Zin / Zout (wideband)	3	3	4
On-Die Passives Integration	2	4	4
Variability / Performance spread	2	4	4
Technology Maturity	5	5	4
Reliability	4	5	5

C. Evolution of RF Performance and the matching network

The necessity for effective power transfer and reduced reflections in different RF systems is what drives the advancement of RF performance and matching networks. Matching networks, sometimes referred to as impedance transformers, are essential for optimising power transmission between a source and a load, like an antenna and a radio frequency (RF) power amplifier. As RF technology develops, so do methods for attaining ideal impedance matching, which enhances the performance of RF systems as a whole.

More sophisticated matching methods have appeared as RF systems became more intricate and run at higher frequencies. These methods include:

i. ***Tunable Matching Networks (TMNs):*** Dynamic impedance matching is made possible by TMNs, allowing for modifications for various operating frequencies or load scenarios (Carr,1981)

ii. ***Multiband Matching Networks:*** For uses such as radio frequency energy harvesting, these networks' ability to match impedance across a larger frequency range is crucial (Clerckx, 2018)

iii. ***Wideband Matching Networks:*** These networks can operate efficiently across a wide variety of frequencies because they are made to match impedance over a big bandwidth.(Akyildiz, 2020)

iv. ***Optimisation Techniques:*** To create matching networks that perform as well as possible under given limitations, optimisation approaches like nonlinear programming are employed.(Bharti, 2022)

Strip lines and stub sections are better suited for networks with operating frequencies higher than 1 GHz. As the frequency increases and the wavelength decreases, the parasitic influence in the discrete elements becomes more apparent and complicates the computation of component values. When the wavelength is sufficiently tiny in relation to the characteristic circuit component length, dispersed components are frequently utilised as an alternative to lumped parts. Since lumped parts are not needed, it is even simple to produce in microstrip or strip line form using a microwave manufacturing aspect. Try to use the shortest transmission line segments to reduce the circuit board's size as shown in figure 8.

Figure 8. Photograph of combined amplification using Strip lines

Impedance changing features of transmission lines, a matching network, a single stub in shunt form, and a balanced stub are all employed. Depending on the impedance requirements, the shunt component may consist of open or short-circuit stub lines. The single counterfoil in shunt form.

D. Evolution of Key Parameters - Noise Figure

Low noise level signal amplification becomes a crucial system requirement for RF amplifiers. Stability and gain are competing criteria in the design of a low noise amplifier as output shown in Figure 9. For example, it is impossible to achieve a minimum noise performance at maximum gain. To perform comparisons and identify tradeoffs between gain and stability, we must devise a technique that enables us to show the impact of noise as a component of the Smith chart.

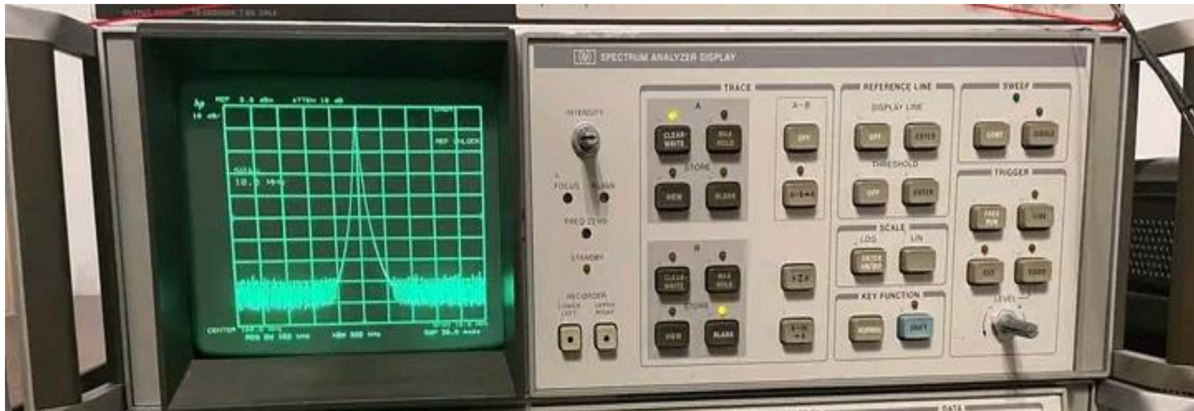

Figure 9. Photograph of Output Noise level

This reduction was achieved by increasing the power density of the technology and reducing the physical dimensions of the drain contact width. For the same power level, the 48-V LDMOS has a substantially lower output capacitance due to the increased power density of the 48-V device. The input capacitance has been kept constant throughout the LDMOS growth by scaling the gate-oxide thickness proportionately to the gate length. The feedback capacitance evolution for 28- and 48-V LDMOS is depicted in Figure 10.

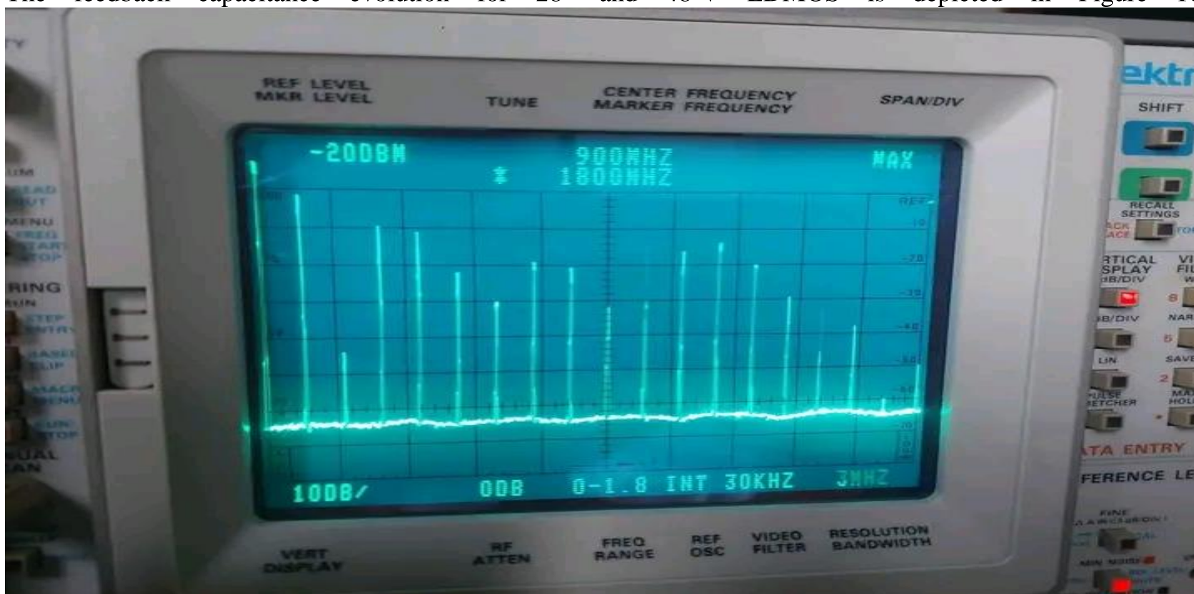

Figure 10. Photograph of capacitance RF feedback output

The on-resistance has improved in tandem with the evolution of the output and feedback capacitance. The most recent 28-V LDMOS and 48-V LDMOS devices normally have on-resistances of 14 and 29 m mm, respectively.

E. Ruggedness Reliability

Apart from the conventional quiescent current degradation and electro-migration robustness, ruggedness is the most crucial reliability metric for RF power devices. Table 2 shown the value of Impact of ruggedness design

changes, because of internal power dissipation, ruggedness failure in MOSFETs is a catastrophic breakdown of the device. It doesn't happen when the device in a power amplifier built using accepted RF design and mechanical engineering concepts operates normally. Impact ionisation, or drain breakdown, is the cause of a MOSFET's toughness failure. The intrinsic gate and drain terminal waveforms drive the internal charge distribution in the MOSFET, which results in the ionisation event. The intrinsic parasitic bipolar NPN transistor in LDMOS is associated with ruggedness. The base resistance and the drain-to-base capacitance are crucial transistor parameters for triggering. Figure 11 shows the CW performance graph with low pass filter versus output power. The drain-source diode drains the excess current to the substrate and clamps the voltage across the parasitic bipolar and the LDMOS. However, the parasitic bipolar transistor may be activated when the drain-source voltage surpasses the diode breakdown voltage due to high sink currents.

Table 2: Impact of ruggedness design changes

Parameter	1 kW Non-Rugged	1 kW Rugged	Improvement Factor
Max Voltage	164V	195V	+18%
ID_{peak}	40A	80A	+100%
Energy Absorbed	1.53J	5.30J	+240%

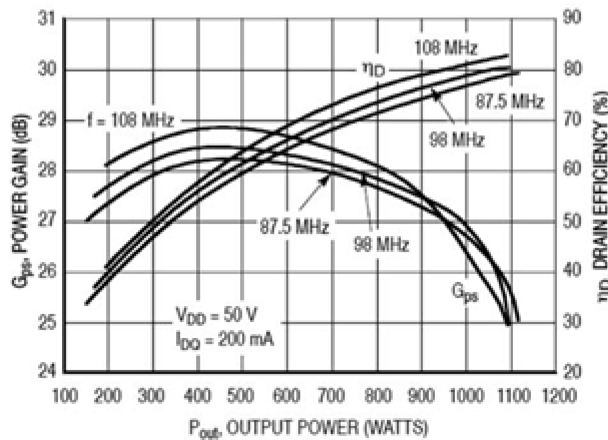

Figure 11. CW performance graph with low pass filter versus output power

IV RF Performance of LDMOS Power Devices

The performance of LDMOS power devices—that is, internally matched devices with peak power levels more than 300 W—is discussed in this section. Figure 12 shows the . RF performance curves circuit performance of push-pull LDMOS. We shall provide the important parameters for Doherty power amplifiers (DPAs) based on the efficiency power contours. Fig. 15 displays the load-pull statistics of a 400-W LDMOS power unit.

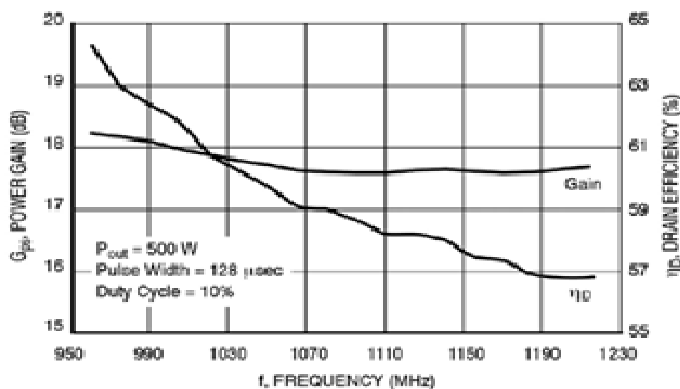

Figure 12. RF performance curves circuit performance

By sweeping the PA device's input power and output load, the efficiency power data is produced. Lower power levels arise from higher output loading situations, while higher power levels often correspond to low output loading conditions. Additionally, the data shown in Figure 13 shows the BLF368 photo with a maximum efficiency of 65% at an output power of 350 W each, which is about 3 dB less than the device's maximum power. Additionally, at power levels below 350 W, the device exhibits a persistent decline in efficiency. At higher power levels, the major loss mechanism is, whereas at lower power levels, the mechanism dominates the loss.

Figure 13. BLF 368 RF LDMOS

For high-efficiency designs like the DPA, the position of the power, efficiency, and gain contour maximum is just as crucial as the LDMOS power device's efficiency and power level. The efficiency, power, and gain curves of the 750-W LDMOS device construction shown in Figure 14. The device's input is conjugate matched and class-AB criteria are enforced (by shorting the harmonics).

Figure 14. Construction of RF LDMOS

The points (loads) for optimal power, efficiency, and gain are arranged in a triangle in actual PA devices, as opposed to a straight line in an ideal high power PA device , RF performance curves, simulated versus measured Pulse width = 128 µsec, duty cycle = 10% as shown in Figure 15. The feedback mechanism, such as the feedback capacitance and source inductance, is the primary cause of these contours' separation in LDMOS devices (under class-AB bias).

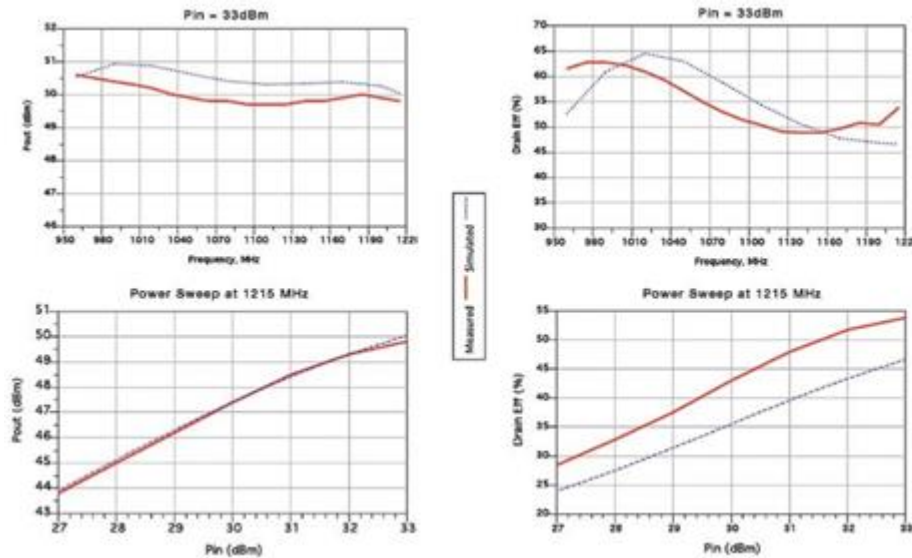

Figure 15. RF performance curves, simulated versus measured
Pulse width = 128 µsec, duty cycle = 10%

V. LDMOS Doherty Implementations

The LDMOS peak efficiency of nearly 70% is located at a power level of 1200 W, or 3-dB push-pull configuration, as shown in the designed module shown in Figure 16. Because the primary device in a two-way DPA is subject to a 3-dB back-off after the power of the entire PA is backed off by 6 dB, this device is advantageous for usage as the main device. Similarly, the load design at 65% efficiency at 4.7-dB back-off power levels (134 W) if the device is utilised as a main device in a three-way DPA configuration. This corresponds to the 9.6-dB back-off of the total PA.

Figure 16. Photograph of RF FM LDMOS Pallet Amplifier

For DPA, the gain of an RF PA is just as crucial as its efficiency. A DPA's gain is dependent on the following three parameters and is lower than the inherent gain of a PA transistor:

i. inherent device gain;
ii. DPA design (e.g., two- or three-way);
iii. variation in gain throughout the DPA's load trajectory.

The contour maxima of the device's power, gain, and efficiency establish the performance parameter; in the DPA design, these maxima should be situated along the load-line trajectory of the primary device (Figure 17).

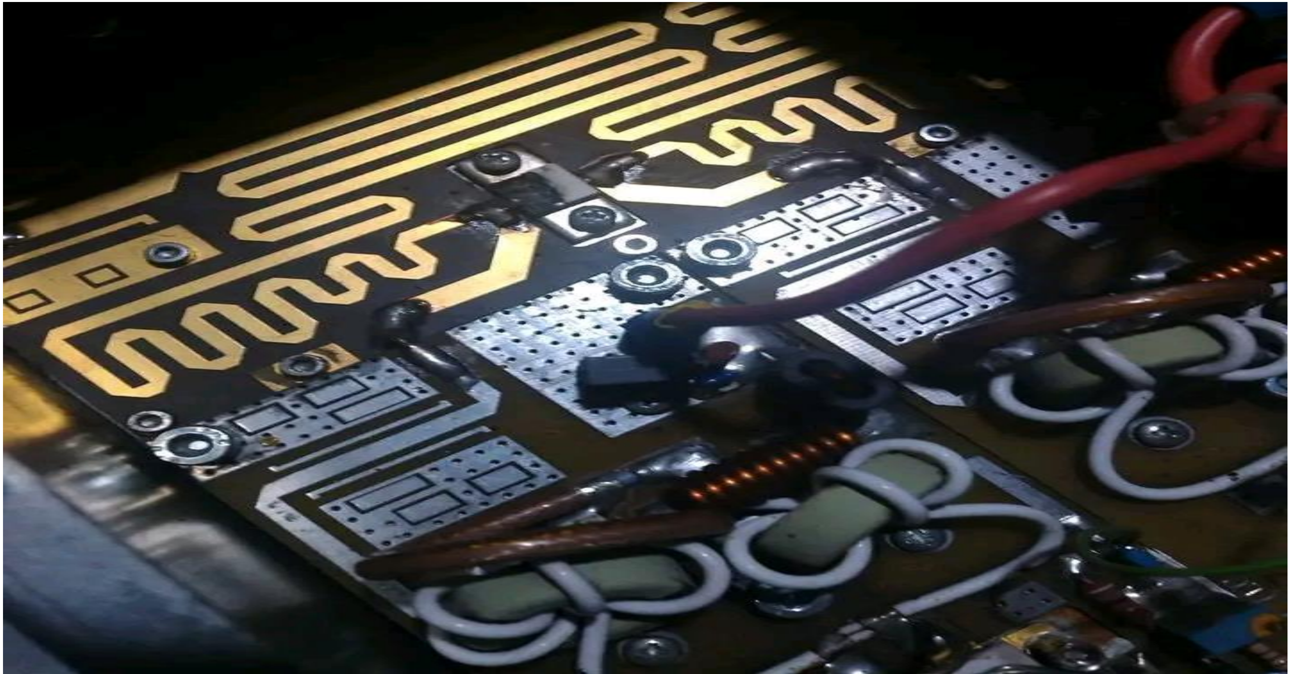

Figure 17. Photograph of RF LDMOS

A picture of a pure carrier without a harmonics filter design is displayed in Figure 18. This amplifier has three 250-W LDMOS semiconductors and is based on the push-pull configuration. The two devices are biased in Class-C mode and serve as peaking devices, while the top device is biased in Class-AB and serves as a primary device. A passive power splitter is used to divide the input power. Only the main PA device is active at deep PBO levels (10 dB), according to the devices' gate biasing.

B. 28-V LDMOS DPAs Results

A picture of a pure carrier without harmonics filter design is displayed in Figure 18. This amplifier has three 250-W LDMOS semiconductors and is based on the push-pull configuration. The two devices at the are biased in Class-C mode and serve as peaking devices, while the top device is biased in Class-AB and serves as a primary device. A passive power splitter is used to divide the input power. Only the main PA device is active at deep PBO levels (10 dB), according to the devices' gate biasing.

Figure 18. Photograph of RF LDMOS

whilst peaking 1 peaking 2 activate at medium dB and high power levels, respectively. A three-way power combiner combines the devices' output power. Figure 19 displays this spectrum three-way LDMOS immediate efficiency.

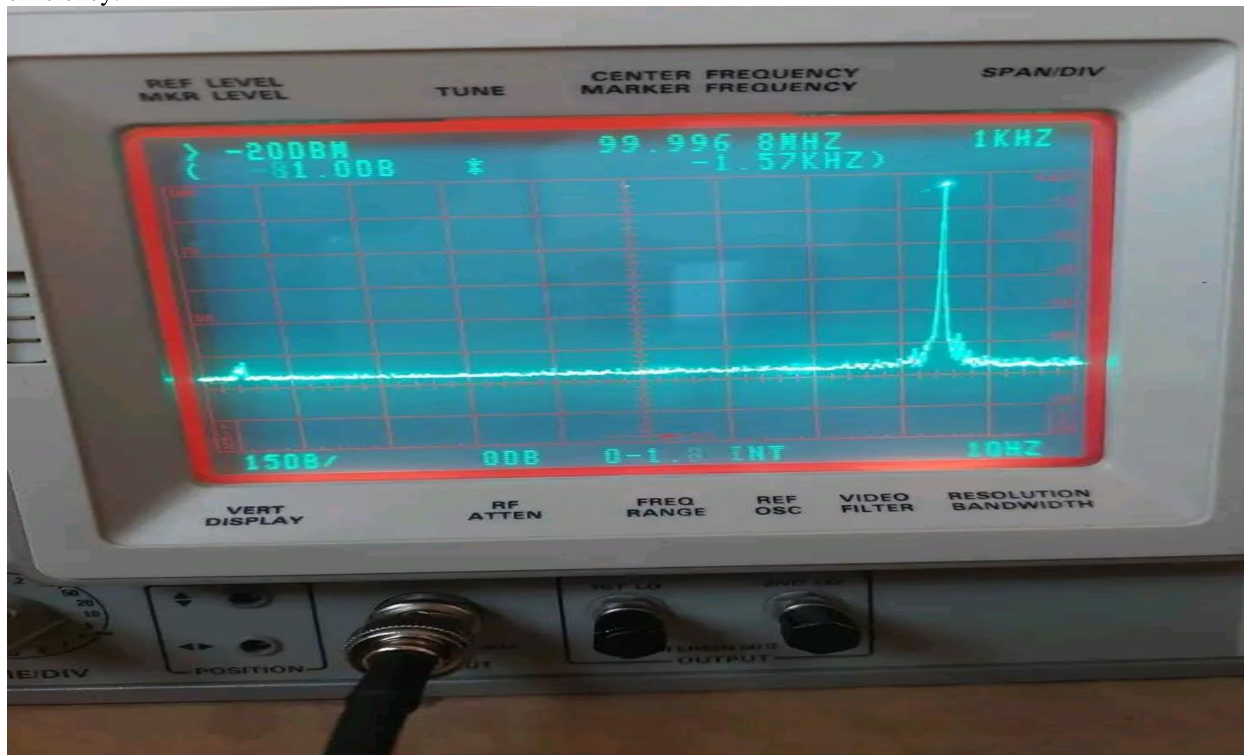

Figure 19. Photograph of RF LDMOS

C. 48 V LDMOS Push-pull Results

Higher RF voltage swings at the PA devices' drain are made possible by 48-V LDMOS technology, which raises the power density and necessary output load values. Due to the lower quality (Q) factor output matching network caused by this high load impedance, the output match's fractional bandwidth increases significantly and losses are reduced. Additionally, a compact output matching network and a denser power packing are made possible by 48-V LDMOS technology, which results in a smaller packaged device. The frequency response of a broadband 88–108 MHz 1500-W LDMOS has a higher efficiency, which represents a 10% improvement over Class AB operation.

VI. CONCLUSION

The RF Power Performance of an LDMOS and applications for FM Broadcast Band II Power Amplifiers are also covered in this study. An analytical model for the surface, vertical, and radial electric field and potential distributions of an M-R LDMOS is also provided. The concurrent optimisation of the M-R LDMOS's surface and vertical electric field distributions can be described rationally. Additionally, all devices having the M-R can use this model. Designers may find the suggested model useful in determining the number and concentration of M-Rs as well as in forecasting the maximum BV of an M-R LDMOS.As demonstrated for a 48-V LDMOS DPA, LDMOS is also appropriate for broadband high-efficiency push-pull amplifiers. Lastly, a 13 dB gain, above 70% efficiency band II – LDMOS amplifier was demonstrated. More sophisticated concepts, such as switching mode amplifiers and -way DPAs, are being made possible by the application of new electromagnetic and device technology concepts to LDMOS technology.

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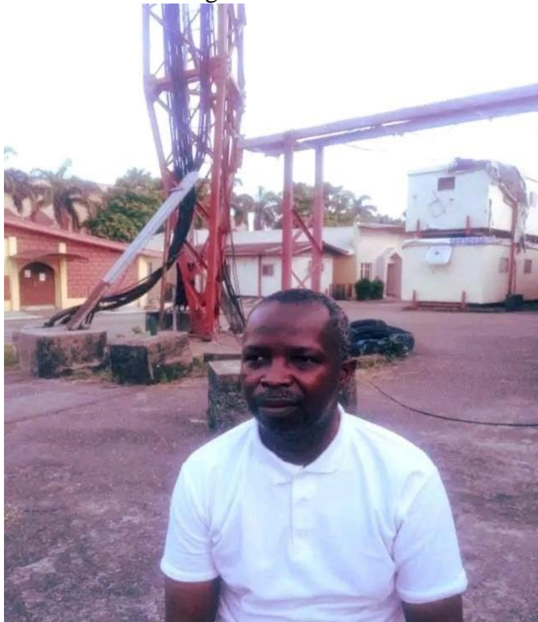

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